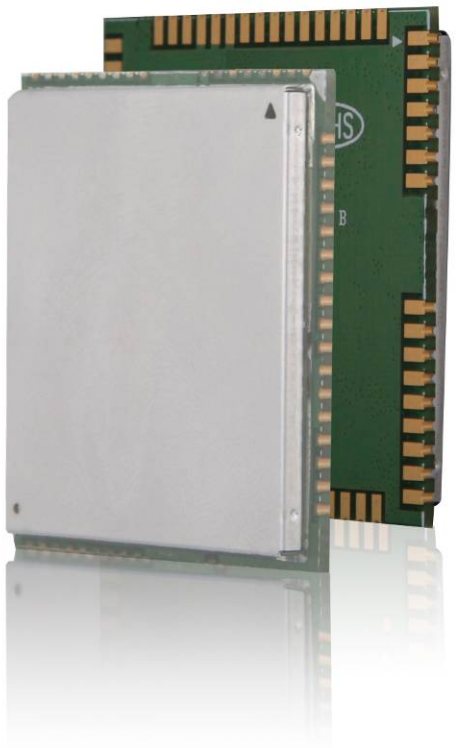
M10

Quectel Cellular Engine

Hardware Design Application Notes

M10_HD_AN01_V1.02



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General Notes

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0. Revision History

Revision	Date	Author	Description of change
1.00	2009-06-25	Ken JI / Samuel HONG	Initial
1.01	2010-02-25	Tracy ZHANG	Modify Figure 1 and Figure 9
1.02	2010-05-30	Yong An	1.Add STATUS pin and its function description 2. Disable VDD_EXT pin as the indication of power-on and power-down.

1. Introduction

This document gives recommendation for Quectel's M10 module integration in a wireless application, such as vehicle tracking system, smart metering and PDA. It gives some recommendations for design notes, reference circuit and PCB layout.

1.1. Related Documents

Table 1: Related documents

SN	Document name	Remark
[1]	M10_HD	Hardware design document of M10 module
[2]	GSM_UART_AN	GSM module UART port application note
[3]	GSM_AUDIO_UGD	GSM module audio design user guide
[4]	GSM_FW_Upgrade_AN01	GSM Firmware upgrade application note

1.2. Terms and Abbreviations

Table 2: Terms and abbreviations

Abbreviation	Description
GPRS	General Packet Radio Service
GSM	Global System for Mobile communications
PCB	Printed Circuit Board
RF	Radio Frequency
SMD	Surface Mounted Devices
SMT	Surface Mount Technology
TCP/IP	Transmission Control Protocol/Internet Protocol

2. Product Concept

The M10 is a Quad-band GSM/GPRS engine that works at frequency bands of GSM850, EGSM 900, DCS1800 and PCS 1900. The M10 features GPRS multi-slot class 12(default)/ class 10/class8 and supports the GPRS coding schemes CS-1, CS-2, CS-3 and CS-4.

The M10 is an SMD type module with 64-pin pads and a tiny profile of 29mm x 29mm x 3. 6 mm (the thickness of PCB is 1.6mm), which can fit into almost all customers' applications. It provides all hardware interfaces between the module and customer's host board.

- External controller can communicate with M10 through its main UART port.
- Two audio channels include two microphone inputs and two speaker outputs, which can be easily configured by AT commands.

The module is designed with power saving technique so that the current consumption could be as low as 0.7mA in SLEEP mode.

TCP/IP and some other Internet protocol stacks have been integrated in the module.

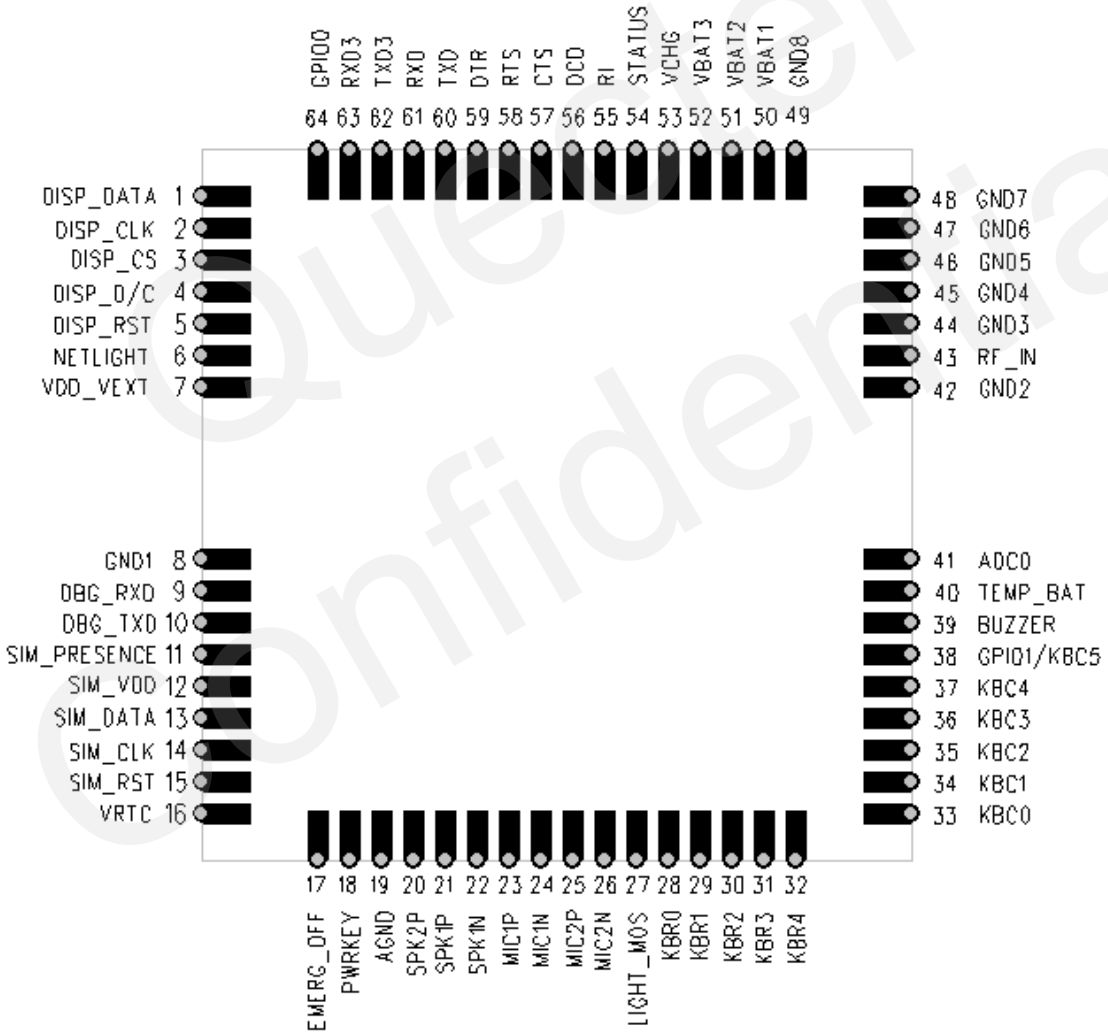
The module is fully RoHS compliant to EU regulation.

3. Placement

Please pay attention to the placement and the PCB layout in your application design.

3.1. Pin Assignment

The pin assignment of the M10 module is shown in Figure 1. Placement of module should be carefully considered to make the RF_IN pad as close as possible to antenna so as to reduce overall RF trace length. The longer the RF trace to antenna, the larger the RF insertion loss. In addition, please keep RF part and antenna from the system crystal and the audio part in host board as far as possible to reduce possible RF interference due to GSM transmission bursts from antenna and RF trace.



VCHG is not supported in the default hardware configuration.

Figure 1: Pin assignment

3.2. Placement Recommendation

The analog part components such as microphone should be placed far away from antenna and power supply. General placement recommendation is shown in Figure 2.

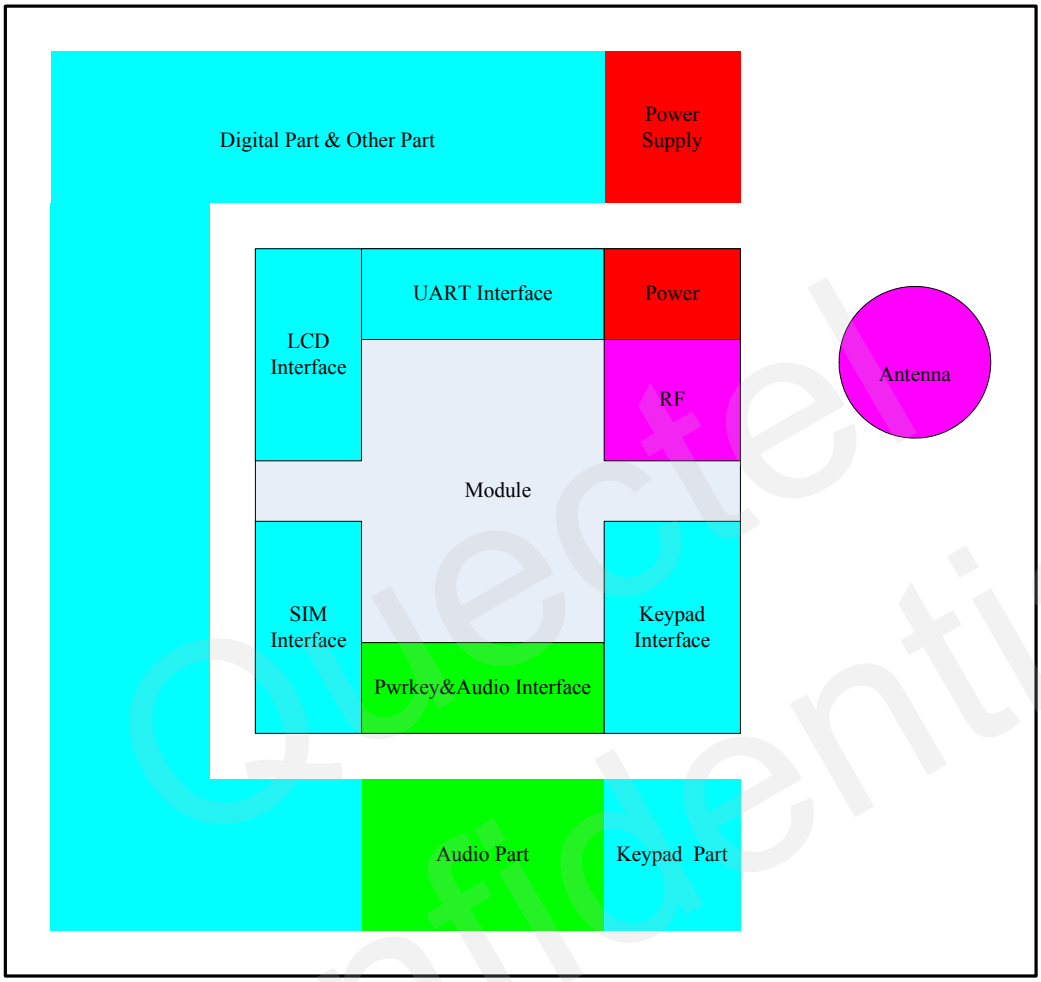


Figure 2: Recommendation of placement

3.3. Placement Clearance

The module mounts with 64 SMT pads. For easy maintenance of this module and accessing to these pads, please keep a distance no less than 3mm between M10 and other components.

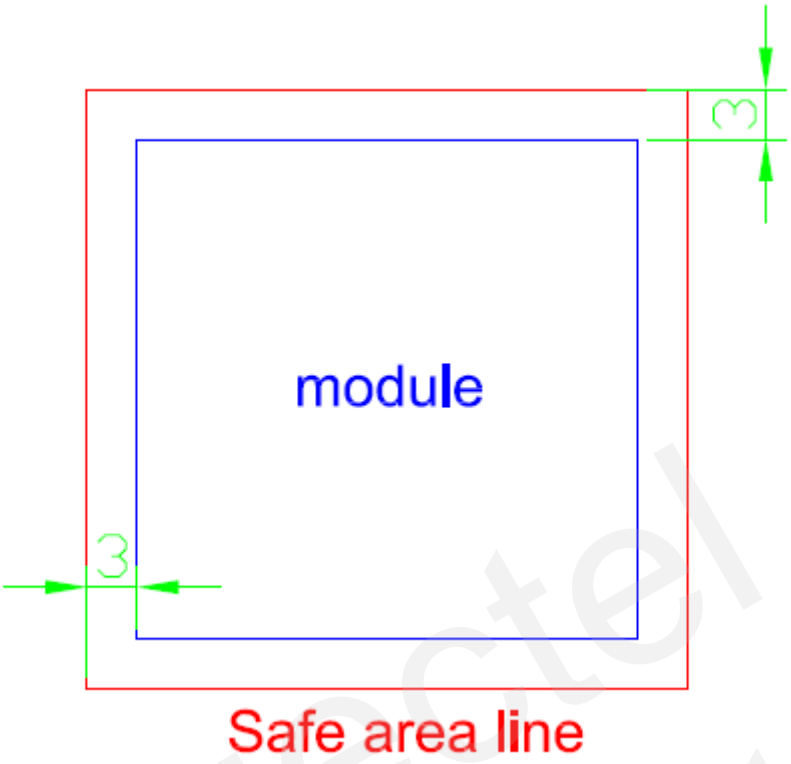


Figure 3: Placement clearance

4. Digital I/O Connection

If the voltage level of peripheral interface circuit does not match module interface, the power consumption of the system could increase, and could even cause the module damaged.

- Each digital I/O of the module operates in a 2.8V logic level inside the module. The voltage level of those digital interfaces connected to the module should match the electrical characteristics of the module listed in Table 3. Otherwise, a level shifter circuit must be inserted between the host and the module.

Table 3: Digital I/O electrical characteristics

SYMBOL	MIN	MAX	UNITS
V_{IL}	0	0.67	V
V_{IH}	1.7	3.1	V
V_{OL}	0	0.34	V
V_{OH}	2.0	2.8	V

- For direct connection between I/Os, please pay attention to I/Os' input or output configuration. If the I/O direction configuration conflicts with each other, the power consumption could increase, and the module could be very hot, and even be damaged. For example, it is forbidden that user's I/O outputs a low level while module's connected I/O outputs a high level.

5. VDD_EXT & STATUS Pin

This pin is a power supply from a regulator inside the module which can power about 20mA of current. Do not use this pin to as indication of power-on and power-off. The STATUS pin can be used to judge whether module is power-on. In customer design, this pin can be connected to a GPIO of DTE or be used to drive an LED in order to judge module operation status. For more details, please refer to Chapter 3.4 in the document [1].

6. Serial Port and Debug Port

The TXD and RXD pins should be connected to host MCU. The DTR pin should be controlled to trigger SLEEP mode or wakeup the module. The RTS and CTS pins should be connected to the host MCU if hardware flow control is required.

The TXD, RXD, PWRKEY and GND pins can also be used for software upgrade and high-level parameters configuration. The DBG_TXD and DBG_RXD pins are only used for software debug. Please note that the PWRKEY pin should be pulled to low level when the M10 is being upgraded. For more detailed information on serial port design, please refer to document [2] and document[3].

Notes: It's recommended to connect the pins necessary for firmware upgrade to external interface.

7. SIM Card

As shown in Figure 4, connecting a large volume capacitor such as 10uF in the SIM_VDD line could lead to failure of detecting the SIM card. A capacitor between 100nF and 1uF is recommended.

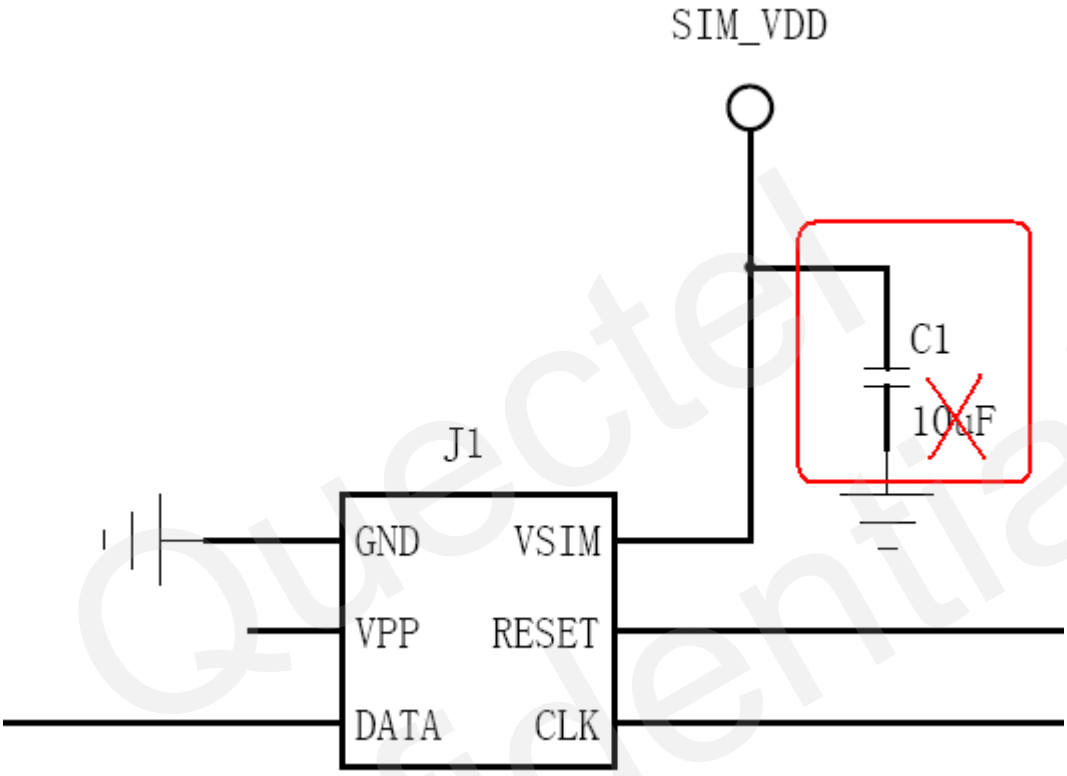


Figure 4: Circuit of the SIM card

8. SLEEP Mode

The command AT+QSCLK can enable or disable SLEEP mode. When the SLEEP mode is enabled, pulling the DTR pin to high level would drive the module into SLEEP mode; and pulling the DTR pin to low level the module would exit from SLEEP mode.

9. Audio Trace

If possible, the audio trace should be placed in inner layer, and shielded by ground in the same layer and the upper and lower adjacent layers to prevent from RF interference. In addition, it is recommended to add as many via as possible between ground layers so as to reduce RF noise.

The AGND signal is usually used for AOUT2 channel to establish a single-end output with SPK2P. Do not pair GND with SPK2P to establish an audio output, otherwise TDD (Time Division Duplex) noise from power supply could occur in AOUT2. For more detailed information on audio design, please refer to document [3].

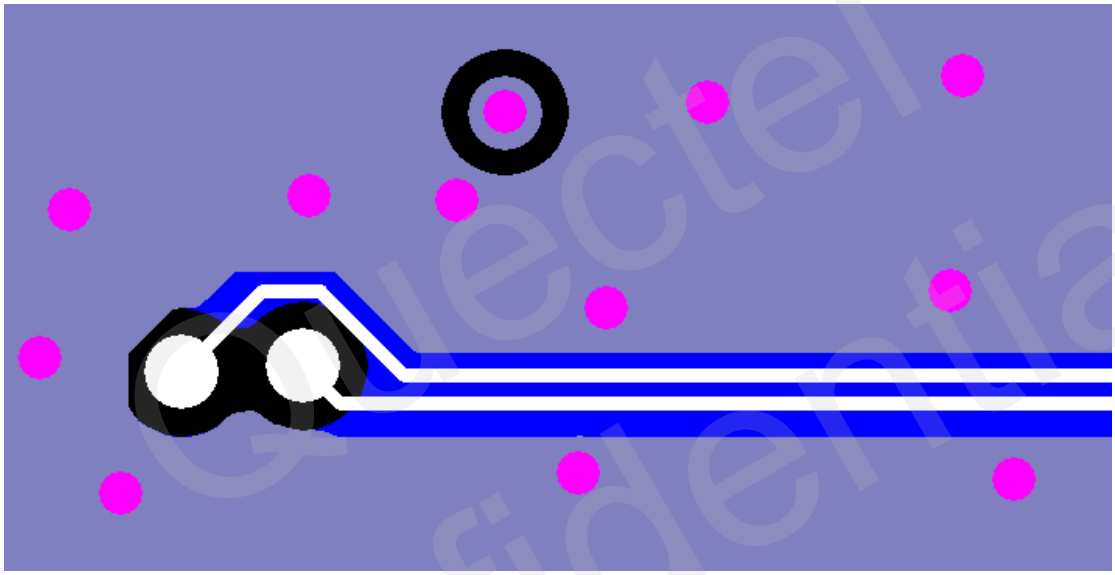


Figure 5: Audio trace routing example

10. RF Design Guide

Correct RF design is essential for RF performance such as TX power, RX sensitivity and harmonics. Following this RF design guide could benefit to improve the RF performance of customer's product.

10.1. Recommended Impedance Matching Circuit

The impedance of M10's RF_ANT port is 50Ω. If the impedance of antenna is close to 50Ω in all working frequency bands, the antenna could be connected to the RF_ANT port directly via 50Ω transmission line. But if the impedance of antenna is not close to 50Ω, a T-type or π-type matching circuit should be inserted between transmission line and antenna. The matching components should be placed as close as possible to the antenna's feed point.

Figure 6 and Figure 7 show the reference designs of T-type and π-type matching circuits.

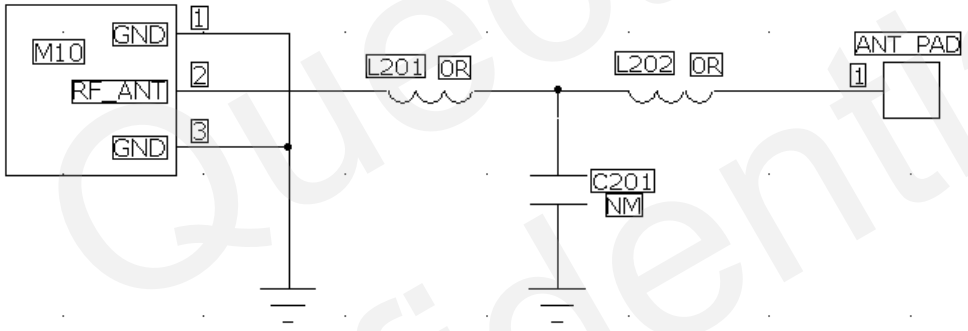


Figure 6: T-type matching circuit

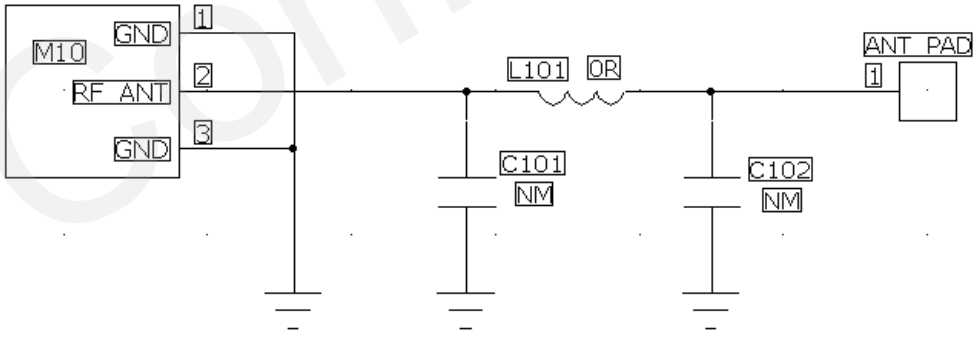


Figure 7: π-type matching circuit

NOTE: The impedance of traces in Bold type must be 50Ω.

10.2. Matched RF Transmission Line Design

In PCB layout, a matched RF transmission line has a fixed characteristic impedance, which is called Z_0, from its source to its load. The source should have an internal resistance of Z_0 and the resistance of matching load should close to Z_0.

Since the impedance of M10's RF_ANT port is 50Ω, the impedance of the RF transmission line from this port to the antenna or the matching circuit should also be made to 50Ω.

More than twelve different types of transmission line can be created on a PCB simply by controlling trace geometry, and some of them are shown in Figure 8.

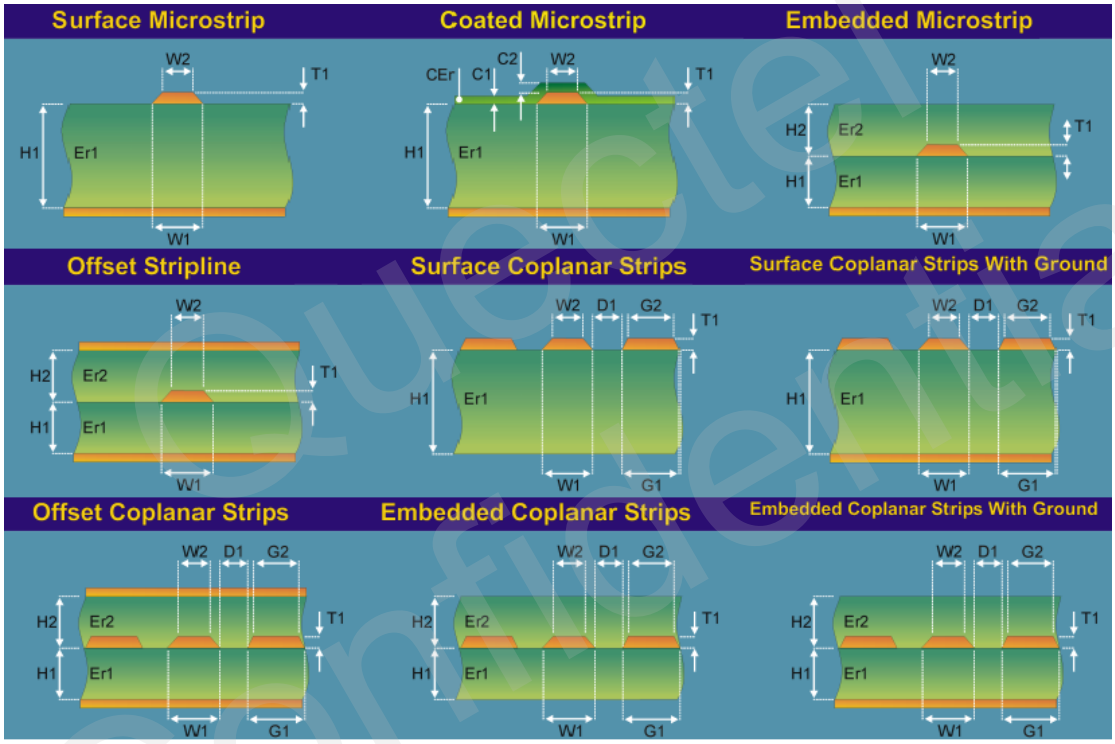


Figure 8: M10 RF_ANT PCB layout

Customer may adopt one or certain types of them to design RF trace. Upon the demand of application design, the number of PCB layer can be different such as two and four. Each type of PCB has corresponding "stack-up". The "stack-up" is the name given to the order of the various etched copper foil and dielectric layers that are laminated together under pressure and heat to make a PCB.

Customer can calculate 50Ω RF trace width by EDA tools such as CITS or APPCAD, or send the "stack-up" to Quectel, and we can help to calculate it.

10.3. PCB Layout Consideration

PCB Layout is essential to the performance of customer's product. Here are some rules that should be followed:

- Impedance control
  Control the impedance of RF trace as close as possible to 50Ω. If the thickness between RF_ANT pad and the ground layer is less than 0.4mm, it could significantly decrease the output power. Therefore, when they are too close, we strongly suggest removing the copper in the layer beneath the RF_ANT pad. If RF trace routes to another layer, add GND via along with it to keep GND integral. The clearance between RF trace and ground plane in same layer should be at least twice the RF trace width.

- Make RF trace as short as possible
  Place the module and the matching circuit near the antenna pad. Shorten the length of RF trace. Place the antenna PAD in the corner or at the edge of host board.

- Protect RF trace
  Avoid placing noise generating traces such as digital signal or clock line near RF trace in the same layer. Carefully route other traces in the layers adjacent to the RF trace, remember not to route in parallel with the RF trace. If possible, keep those traces far away from the RF trace.

- An RF test point is located at the bottom side of M10 for manufacture purpose. The copper which is close to this test point in the top layer of customer's host board must be kept out or removed. No signal trace should be placed in the top layer and the second layer beneath this test point. The location of the test point and the size of removed copper are as Figure 9.

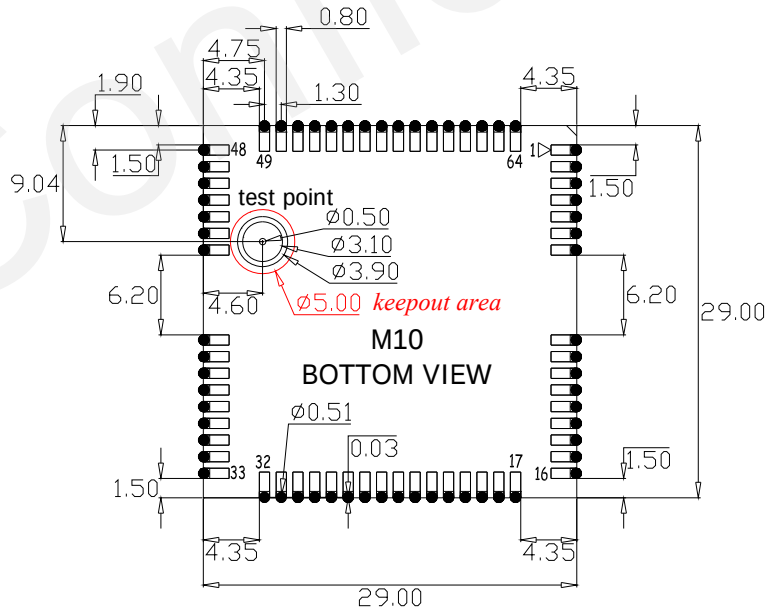


Figure 9: M10 bottom dimensions

- Customer can use either antenna PAD or RF connector to connect the antenna. If antenna PAD is adopted, Figure 10 is a reference design for a four-layer PCB. Make the space on all layers beneath antenna pad keep-out. Place a ground PAD near the antenna PAD. The distance between GND PAD and antenna PAD can be around 1.8mm. The size of antenna PAD can be 1.8mm*1.8mm, and the GND PAD should be a little bigger, e.g. 2.5mm*2.5mm. Add several GND via near or on the GND PAD to reduce impedance from the GND PAD to the RF reference ground.

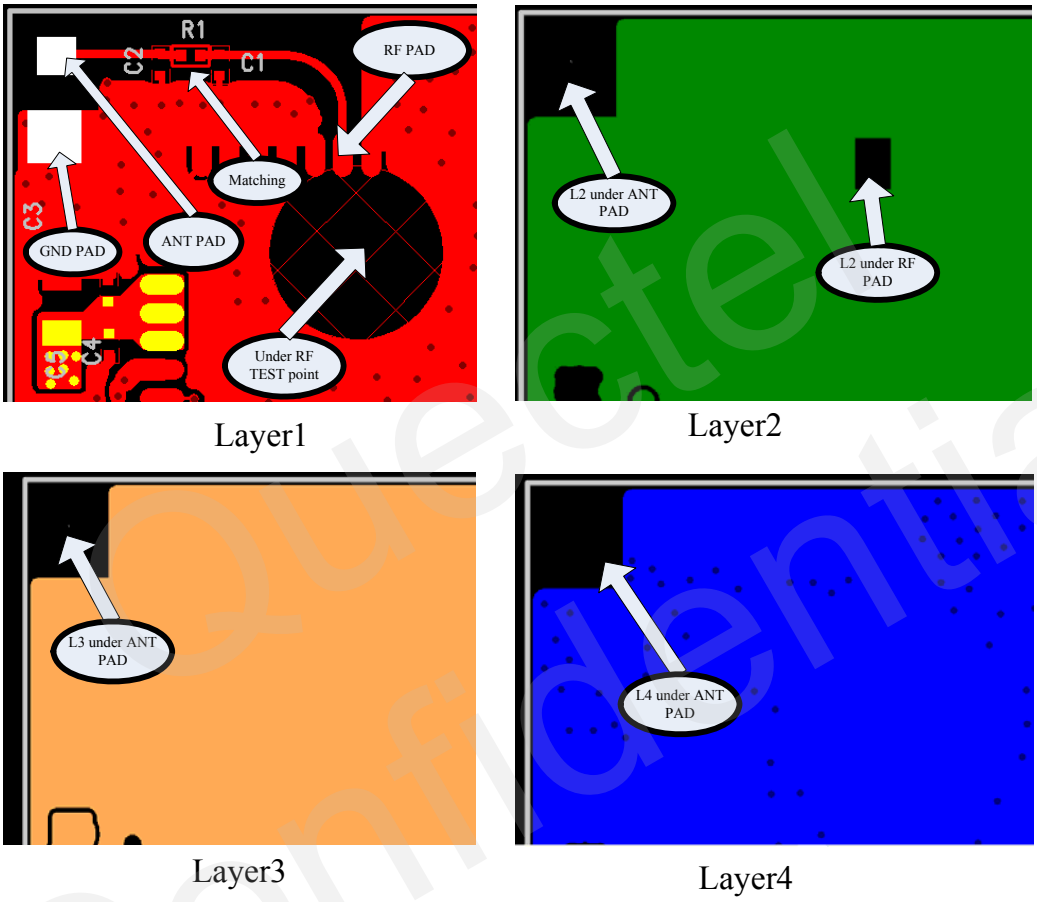


Figure 10: Reference PCB design with antenna pad in a four-layer PCB

If RF connector is adopted, place the RF connector close to module RF_ANT, and add several ground via close to the GND PAD of RF connector. Figure 11 is the reference PCB design.

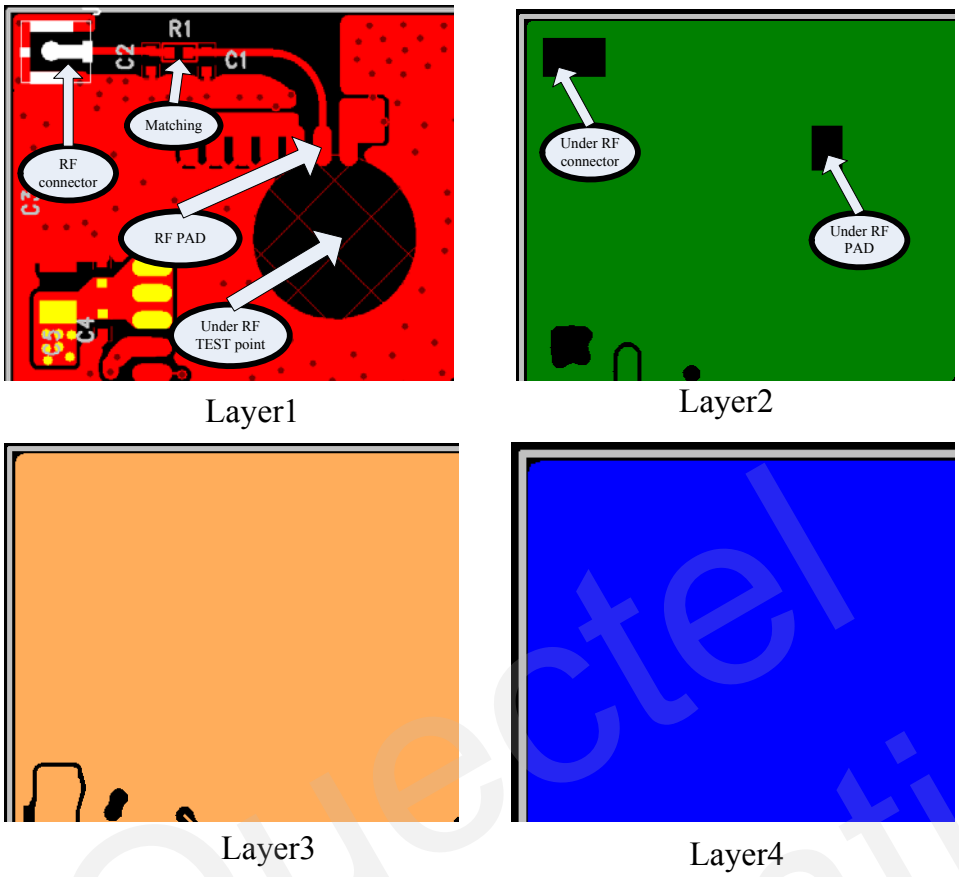


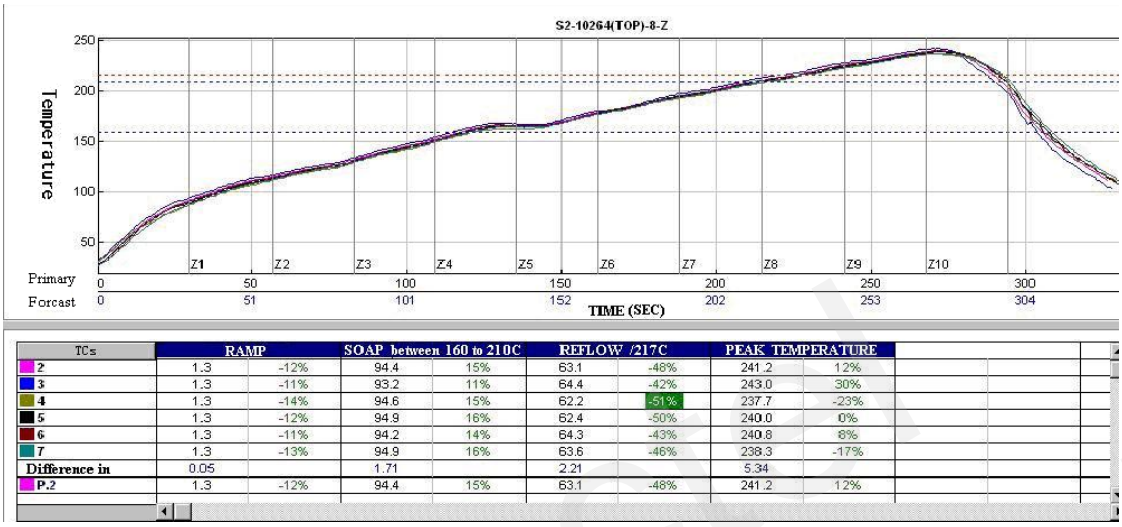
Figure 11: Reference PCB design with RF connector in a four-layer PCB

The stack-up of the four-layer PCB is shown in Table 4.

Table 4: Stack-up of the four-layer PCB

	Solder Mask	18.0 µm.	
	Chemical Gold	0.05 µm.	
	Electroless Nickel	2.54 µm.	
	Copper Plating	13 µm.	
LAYER1	Copper	12.0 µm.	
	1080LDP	200.0 µm	standard-vias 1-4
LAYER2	Copper	18.0 µm.	
	Prepreg 2116	500.0 µm.	
LAYER3	Copper	18.0 µm.	
	1080LDP	200.0 µm.	
LAYER4	Copper	12.0 µm.	
	Copper Plating	13 µm.	
	Electroless Nickel	2.54 µm.	
	Chemical Gold	0.05 µm.	
	Solder Mask	18.0 µm.	

11. The Recommended Ramp-soak-spike Reflow Profile



TCs	RAMP		SOAP between 160 to 210C		REFLOW /217C		PEAK TEMPERATURE	
2	1.3	-12%	94.4	15%	63.1	-48%	241.2	12%
3	1.3	-11%	93.2	11%	64.4	-42%	243.0	30%
4	1.3	-14%	94.6	15%	62.2	-51%	237.7	-23%
5	1.3	-12%	94.9	16%	62.4	-50%	240.0	0%
6	1.3	-11%	94.2	14%	64.3	-43%	240.8	8%
7	1.3	-13%	94.9	16%	63.6	-46%	238.3	-17%
Difference in	0.05		1.71		2.21		5.34	
P.2	1.3	-12%	94.4	15%	63.1	-48%	241.2	12%

Figure 12: The recommended ramp-soak-spike reflow profile

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