UC20&M10 Reference Design Explanation

1. The difference on the interface between UC20 and M10.

Refer to the document <UC20&M10_Compatibility_Design> for more details.

2. The explanation of compliant footprint.

Refer to the document <UC20_Hardware_Design> and our reference footprint for more details.

3. The difference on the voltage level between UC20 and M10.

	VBAT	VDD_EXT	VRTC	PWRKEY	RESET_N/EMERG_OFF	NET_STATUS/NETLIGHT	ADC	UART	ANT_MAIN
UC20	3.4~4.3	1.8	1.5~3.2	1.8	1.8	1.8	0.2~2.1	1.8	GSM+WCDMA
M10	3.3~4.6	2.8	1.5~3.3	VBAT	2.8	2.8	0~2.8	2.8	GSM Quad-band

4. The explanation of compliant circuit.

Refer to the related sheet for details.

5. Index of reference design.

Sheet 1: Design Explanation

Sheet 2: Module Interface

Sheet 3: Power Supply Design

Sheet 4: UART and SIM Design

Sheet 5: Audio Design

Sheet 6: RF and GPS Design

Sheet 7: Other Designs

Sheet 8: MCU Interface

| Quectel Wireless Solutions		
DRAWN BY <Mountain.ZHOU>	PROJECT <UC20&M10 Reference Design>	TITLE <Design Explanation>
CHECKED BY <Bruce.YU>	SIZE A2	VER 1.01
	SHEET 1 of 8	<2013.04>

Module Interface

U201-A UC20&M10

Signal labels (top):
GND · USB_VBUS · USB_DM · USB_DP · RXD · TXD · DTR · RTS · CTS · DCD · RI · STATUS · VBAT_BB · VBAT_BB · VBAT_RF · VBAT_RF · GND · BOOT_KEY

USB_VBUS [7,8] · USB_DM[7,8] · USB_DP[7,8] · RXD[4,7] · TXD[4,7] · DTR[4] · RTS[4] · CTS[4] · DCD[4] · RI[4] · STATUS[7] · VBAT_BB[3] · VBAT_RF[3] · BOOT_KEY[7]

R216 0R · R215 0R · R214 0R · R213 0R

Pin numbers top: 72 71 70 69 68 67 66 65 64 63 62 61 60 59 58 57 56 55

Left side pins U201-A:
- 1 RESERVED
- 2 RESERVED
- 3 RESERVED
- 4 RESERVED
- 5 NET_MODE — [7] NET_MODE
- 6 NET_STATUS — [2,7] NET_STATUS
- 7 VDD_EXT — [2,4,5] VDD_EXT
- 8 GND
- 9 GND
- 10 SIM_GND — [2,4] SIM_GND
- 11 DBG_RXD — [2,7] DBG_RXD
- 12 DBG_TXD — [2,7] DBG_TXD
- 13 SIM_PRESENCE — [2,4] SIM_PRESENCE
- 14 SIM_VDD — [2,4] SIM_VDD
- 15 SIM_DATA — [2,4] SIM_DATA
- 16 SIM_CLK — [2,4] SIM_CLK
- 17 SIM_RST — [2,4] SIM_RST
- 18 VRTC — [2,3] VRTC

Right side pins U201-A:
- 54 GND
- 53 GND
- 52 GND
- 51 GND
- 50 GND
- 49 ANT_MAIN — ANT_MAIN [6]
- 48 GND
- 47 ANT_GPS — ANT_GPS [6]
- 46 GND
- 45 ADC0 — ADC0 [7]
- 44 ADC1 — ADC1 [7]
- 43 RESERVED
- 42 I2C_SDA — R211 0R — I2C_SDA [5]
- 41 I2C_SCL — R212 0R — I2C_SCL [5]
- 40 RESERVED
- 39 RESERVED
- 38 RESERVED
- 37 RESERVED

Bottom pins U201-A:
19 GND · 20 RESET_N · 21 PWRKEY · 22 AGND · 23 RESERVED · 24 PCM_IN · 25 PCM_OUT · 26 PCM_SYNC · 27 PCM_CLK · 28 RESERVED · 29 RESERVED · 30 RESERVED · 31 RESERVED · 32 RESERVED · 33 RESERVED · 34 GPS_VDD · 35 ANT_DIV · 36 GND

[2]RESET_N · [2,7]PWRKEY

R209 0R — ANT_DIV [6]
R210 0R — GPS_VDD [6]
R201 0R / R202 NM_0R — PCM_CLK [5] / MIC1N [5]
R203 0R / R204 NM_0R — PCM_SYNC [5] / MIC1P [5]
R205 0R / R206 NM_0R — PCM_OUT [5] / SPK1P [5]
R207 0R / R208 NM_0R — PCM_IN [5] / SPK1N [5]

U201-B UC20&M10

Top pins: 112 111 110 109 108 107 106 105 — GND (all)

Left pins:
- 73 RESERVED
- 74 RESERVED
- 75 RESERVED
- 76 RESERVED
- 77 RESERVED
- 78 RESERVED
- 79 RESERVED
- 80 RESERVED
- 81 RESERVED
- 82 RESERVED
- 83 RESERVED
- 84 RESERVED

Right pins:
- 104 GND
- 103 GND
- 102 GND
- 101 GND
- 100 GND
- 99 GND
- 98 GND
- 97 GND
- 96 GND
- 95 GND
- 94 GND
- 93 GND

Bottom pins: 85 86 87 88 89 90 91 92 — GND (all)

U201-C UC20&M10

Left pins:
- 113 M10:SD_DATA
- 114 M10:SD_CLK
- 115 M10:SD_CMD
- 116 M10:RESERVED
- 117 M10:RESERVED
- 118 M10:NETLIGHT — [2,7] NET_STATUS
- 119 M10:VDD_EXT — [2,4,5] VDD_EXT
- 120 M10:GND — [2,4] SIM_GND

Right pins:
- M10:DBG_RXD — 121 — DBG_RXD [2,7]
- M10:DBG_TXD — 122 — DBG_TXD [2,7]
- M10:SIM_PRESENCE — 123 — SIM_PRESENCE [2,4]
- M10:SIM_VDD — 124 — SIM_VDD [2,4]
- M10:SIM_DATA — 125 — SIM_DATA [2,4]
- M10:SIM_CLK — 126 — SIM_CLK [2,4]
- M10:SIM_RST — 127 — SIM_RST [2,4]
- M10:VRTC — 128 — VRTC [2,3]

When M10 is applied, SIM_GND connects to M10 GND pin.

For UC20, it is used to reset the module.
For M10, it is EMERG_OFF used to turn off the module.
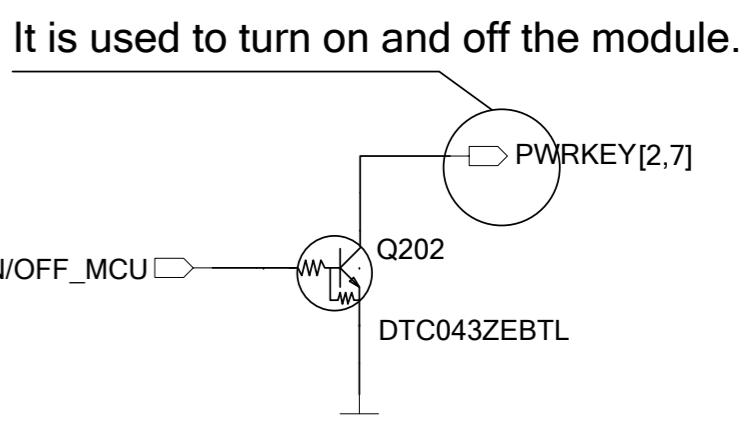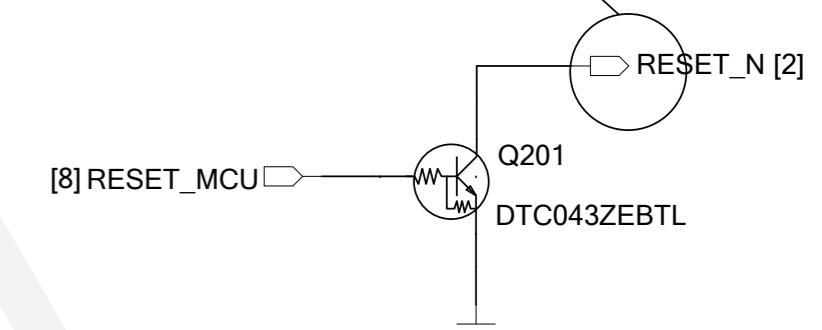
[8] RESET_MCU — Q201 DTC043ZEBTL — RESET_N [2]

It is used to turn on and off the module.

[8] ON/OFF_MCU — Q202 DTC043ZEBTL — PWRKEY[2,7]

Notes:

1. The SMD difference between UC20 and M10.

Intended audience	Installed	Not installed
M10	R202, R204, R206, R208	R201, R203, R205, R207, R209~R216
UC20	R201, R203, R205, R207, R209~R216	R202, R204, R206, R208

2. Please refer to sheet 1 and M10 and UC20 Hardware Design respectively for further details about the difference between them.

3. Keep all reserved pins open.

Power Supply Design

LDO Application

It is used when the input voltage is below 7V.

+ 5V

DC_IN

U301 MIC29302BU

C301 100uF C302 100nF

2 IN OUT 4 VBAT

1 EN 3 GND 5 ADJ

R301 51K

R302 100K 1%

C303 100uF C304 75pF C305 15pF

R303 47K 1%

$VBAT = (R302/R303+1)*1.24 = 3.88V$

VRTC Design

[2] VRTC

B301 XH414

C313 + NM_100uF
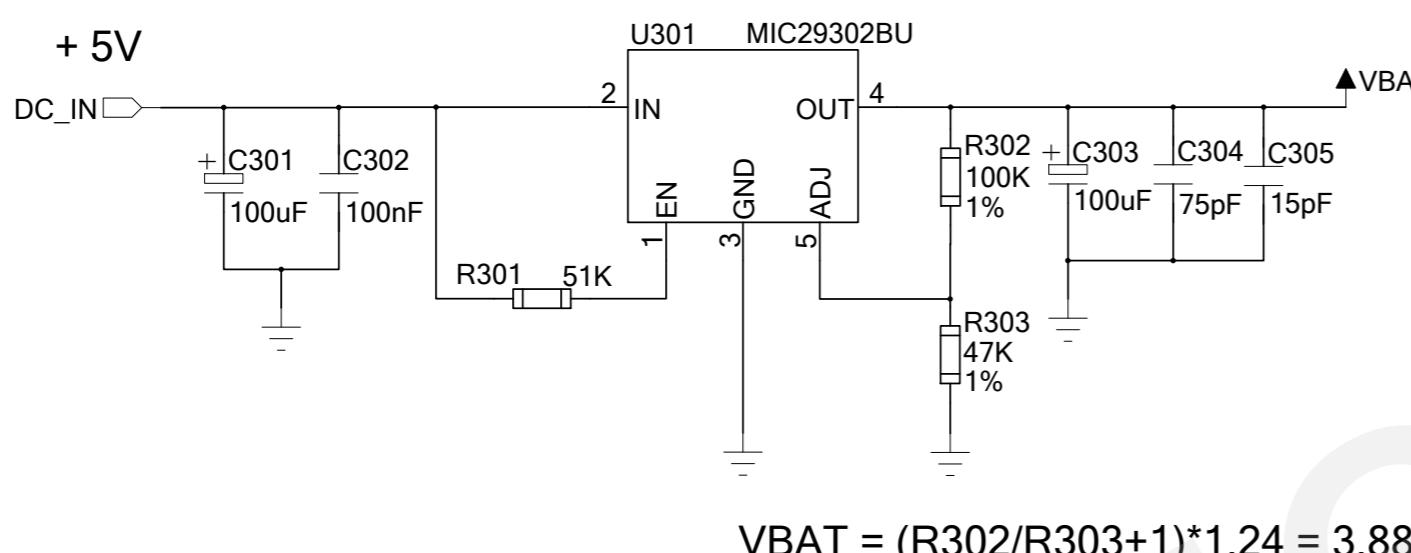
If not used, keep this open.
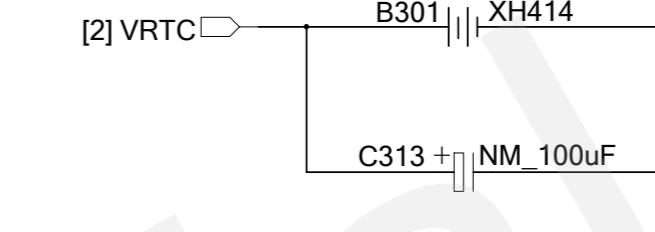
DC-DC Application

1. It is used when the input voltage is above 9V in the vehicle application.

2. Use DC-DC to convert high input voltage to 5V,

   and LDO will generate 3.8V typical voltage for the module.

e.g. DC12V IN → DC-DC → DC 5V out → LDO → DC 3.8V out for module
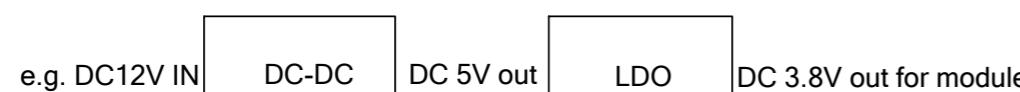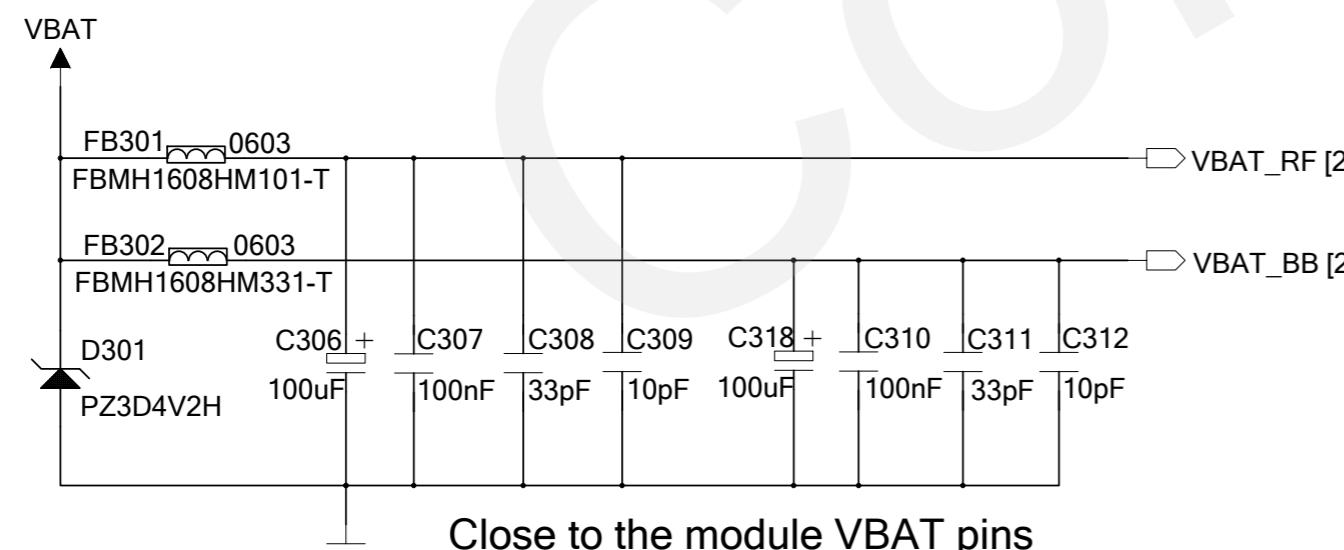
Power for PCM Codec and ADC Circuit
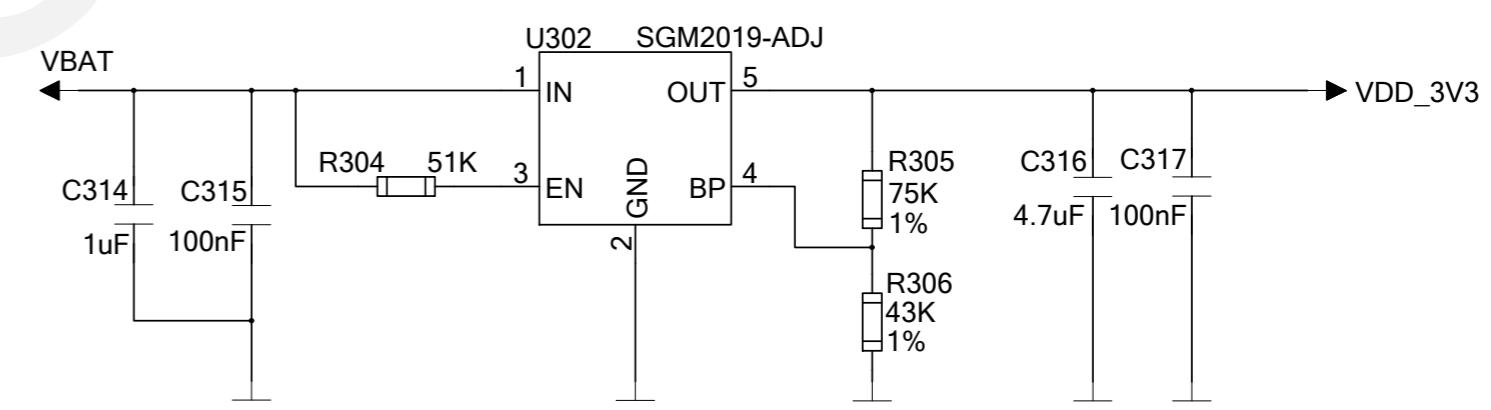
VBAT

U302 SGM2019-ADJ

C314 1uF C315 100nF

R304 51K

1 IN OUT 5 VDD_3V3

3 EN 2 GND BP 4

R305 75K 1%

C316 4.7uF C317 100nF

R306 43K 1%

$Vout = (R305/R306+1)*1.207 = 3.3V$

VBAT Design

VBAT

FB301 0603
FBMH1608HM101-T

VBAT_RF [2]

FB302 0603
FBMH1608HM331-T

VBAT_BB [2]

D301
PZ3D4V2H

C306 + 100uF C307 100nF C308 33pF C309 10pF C318 + 100uF C310 100nF C311 33pF C312 10pF

Close to the module VBAT pins

Notes:

1. VBAT should be routed in star mode to VBAT_BB and VBAT_RF net.

2. The rated current of FB301 and FB302 should be more than 1.6A.

UART and SIM Design

UART Level Translator

U401 TXB0108PWR

Pin	Signal		Pin	Signal
1	A1	B1	20	
2	VCCA	VCCB	19	
3	A2	B2	18	RI_M [8]
4	A3	B3	17	DCD_M [8]
5	A4	B4	16	RTS_M [8]
6	A5	B5	15	RXD_M [8]
7	A6	B6	14	DTR_M [8]
8	A7	B7	13	CTS_M [8]
9	A8	B8	12	TXD_M [8]
10	OE	GND	11	

R401 51K, R402 51K, R403 10K, R404 120K
C401 100nF, C402 100nF

VDD_EXT, VDD_MCU
[2] RI, [2] DCD, [2] RTS, [2,7] RXD, [2] DTR, [2] CTS, [2,7] TXD
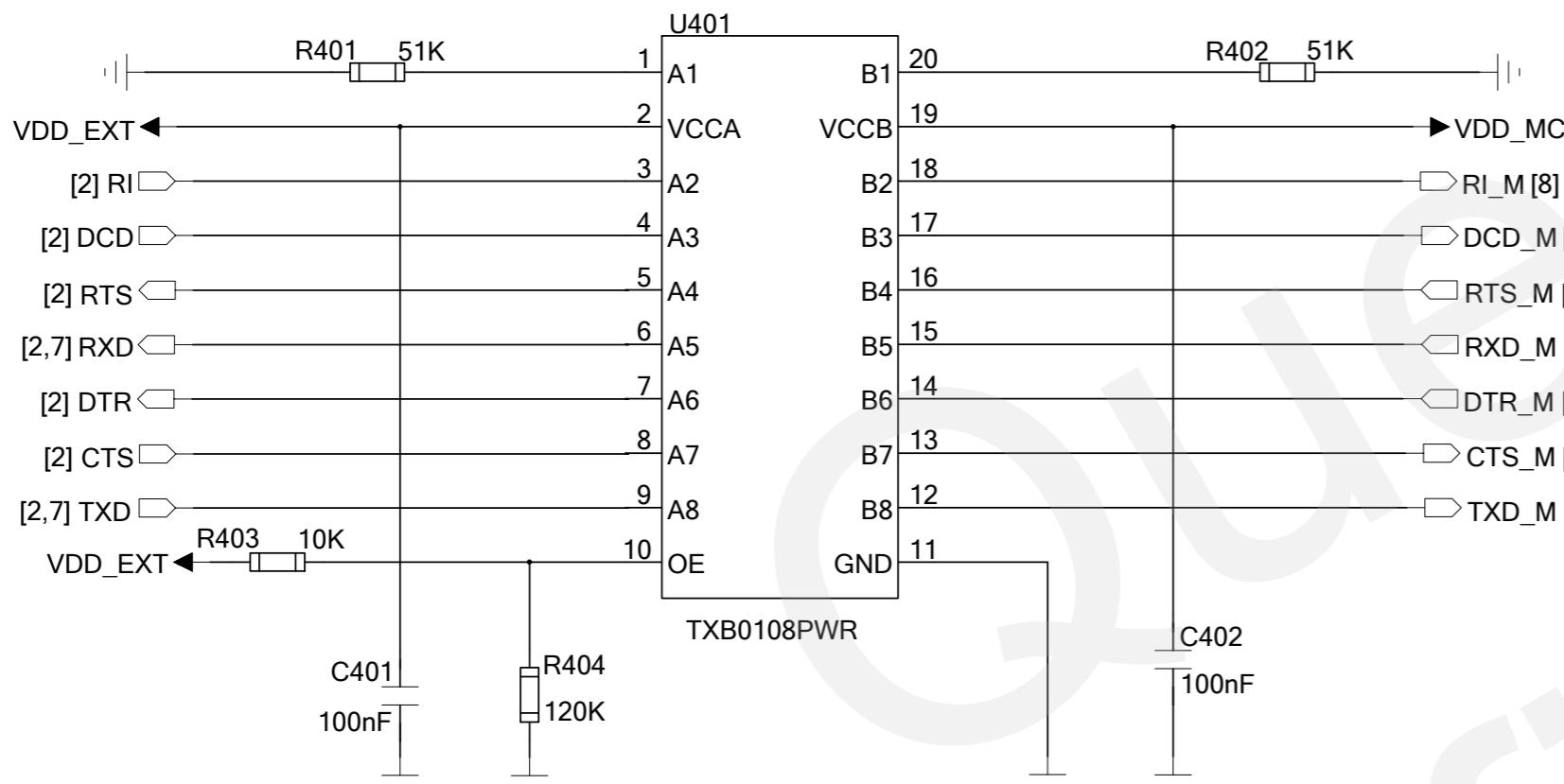
Notes:

1.TXB0108 is to realise the voltage level translation between UC20/M10 and MCU.

2.This circuit is available for both UC20 and M10 UART voltage level translation design.

3.VCCA should not exceed VCCB.

   For more information about TXB0108, please refer to the datasheet.

SIM Design

J401 Molex 91228

Signal		Signal
VCC		GND
RST		VPP
CLK		I/O
PRESENCE		

SIM_VDD, SIM_VDD, VDD_EXT
R408 NM_15K, R409 51K
C406 100nF
[2]SIM_RST R405 22R
[2] SIM_CLK R406 22R
[2] SIM_PRESENCE
[2] SIM_DATA R407 22R
SIM_GND [2]
C403 33pF, C404 33pF, C405 33pF
U402 ESDA6V8AV6
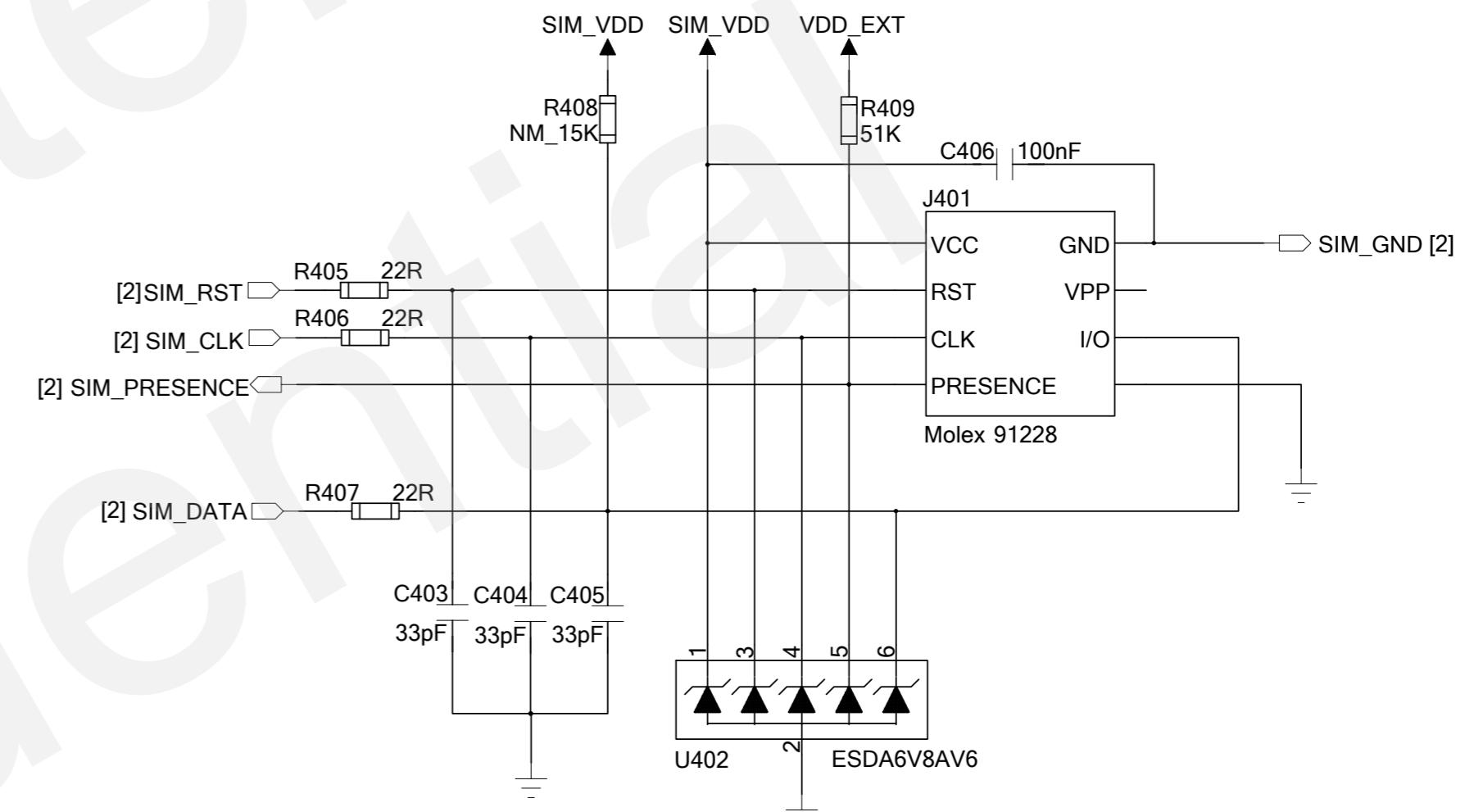
Notes:

1.R405~R407 are applied to suppress the EMI spurious transmission

   and enhance the ESD protection.

2.R408 is reserved to improve anti-jamming capability for long SIM_DATA layout trace.

3.SIM_PRESENCE is used to detect SIM card, which will be low when the SIM card is inserted.

   This function on UC20 is not supported currently.

4.The value of C406 should be less than 1uF.

Audio Design

## PCM Codec Circuit

U501 NAU8814

- 24 MIC+
- 23 MIC-
- 22 VREF
- 21 AUX
- 20 VDDSPK
- 19 SPKOUT-
- 18 VSSSPK
- 17 SPKOUT+
- 16 MOUT
- 15 MODE
- 14 SDIN
- 13 SCLK
- 25 AGND
- 1 MICBIAS
- 2 VDDA
- 3 VSSA
- 4 VDDC
- 5 VDDB
- 6 VSSD
- 7 ADCOUT
- 8 DACIN
- 9 FS
- 10 BCLK
- 11 MCLK
- 12 CS

[5] MIC- / [5] MIC+

[5] MICBIAS — 1 MICBIAS
[5] VDDA — 2 VDDA
VDD_EXT — 4 VDDC
VDD_3V3 — 5 VDDB

C512 4.7uF

R510 0R → VDD_3V3
C511 10uF
C510 4.7uF
C509 100nF

SPK1N [2,5]

VSSSPK (18)
SPKOUT+ (17) → SPK1P [2,5]
MOUT (16) → VDD_EXT
MODE (15) R509 10K R507 10K R508 10K
SDIN (14) → I2C_SDA [2]
SCLK (13) → I2C_SCL [2]

C501 4.7uF C502 100nF C503 4.7uF C504 100nF

[2] PCM_IN — R501 22R
[2] PCM_OUT — R502 22R
[2] PCM_SYNC — R503 22R
[2] PCM_CLK — R504 22R

R505 0R R506 10K

C505 NM C506 NM C507 NM C508 22pF

[5] MICBIAS — R512 0R
C515 100nF C516 4.7uF
R513 1K
R514 1.5K

[5] MIC+ — C517 1uF — MIC1P [2,5]
C519 10uF
[5] MIC- — C518 1uF — MIC1N [2,5]
R515 1.5K
R516 1K

VDD_3V3 — R511 0R — VDDA [5]
C513 4.7uF C514 100nF

This circuit is available for UC20 audio applicaion only.

Audio Channel - Earphone

[2,5] MIC1N
[2,5] SPK1P — C535 22uF
C536 NM C537 10pF C538 33pF

C532 10pF C533 33pF C534 4.7uF   Close to earphone interface

J502
[2,5] MIC1P
C539 10pF C540 33pF D505 D506 PESD5V0S1BL
3 / 4 / 2 / 1 Earphone

R517 0R

Audio Channel - Handset

C520 10pF C521 33pF C522 10pF C523 33pF C524 10pF C525 33pF D501 D502 PESD5V0S1BL

J501
[2,5] MIC1P — 4
[2,5] MIC1N — 1
[2,5] SPK1P — 3
[2,5] SPK1N — 2
HANDSETCON

C526 10pF C527 33pF C528 10pF C529 33pF C530 10pF C531 33pF D503 D504 PESD5V0S1BL

RF and GPS Design

Main Antenna Interface

J601 Main Antenna

R601 0R

ANT_MAIN [2]

C601
NM

L601
NM
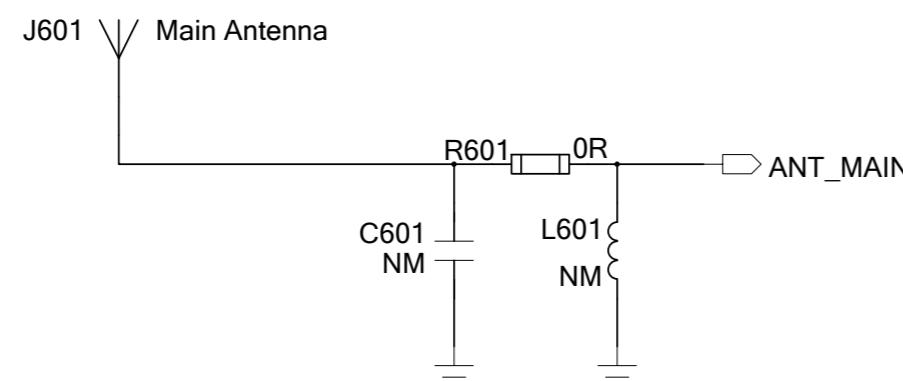
Diversity Antenna Interface

J602 Diversity Antenna

R602 0R

ANT_DIV [2]

C602
NM

L602
NM
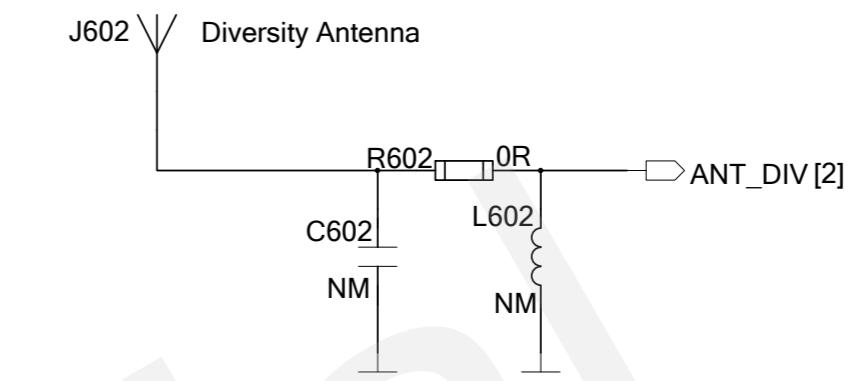
ANT_DIV is used to improve RF signal reliability and quality.

GPS LNA Circuit

GPS_VDD

Care must be taken that GPS_VDD circuit only supplies power for active antenna.

C603
0.1uF

R603
10R

J603
GPS Antenna

L603
56nH

C604 100pF

GPS_IN [6]

D601
LXES15AAA1-100

GPS_VDD

C606 220nF

C607 33pF
R604 51K

[6] GPS_IN

L604 6.8nH

U601
1 GND   VCC 4
2 GND   SHDN 5
3 RFIN   RFOUT 6
MAX2659

R605 NM_0R

GPS_LNA_EN [8]

C605
NM

C608 56pF

C609
NM

ANT_GPS [2]
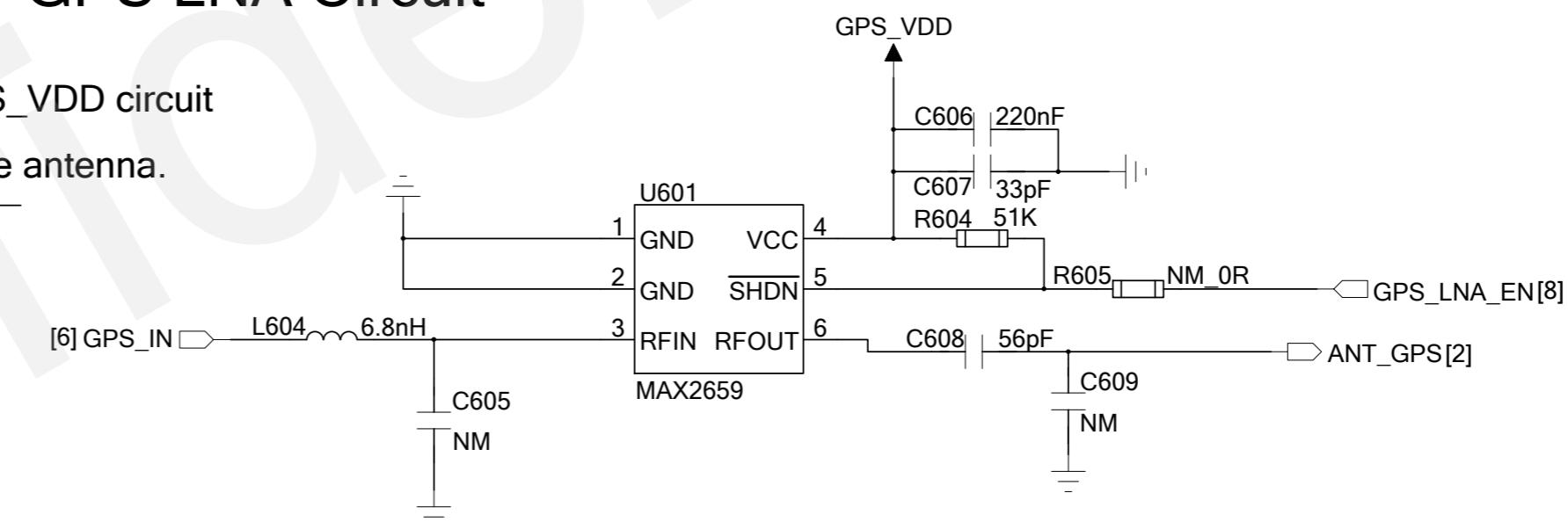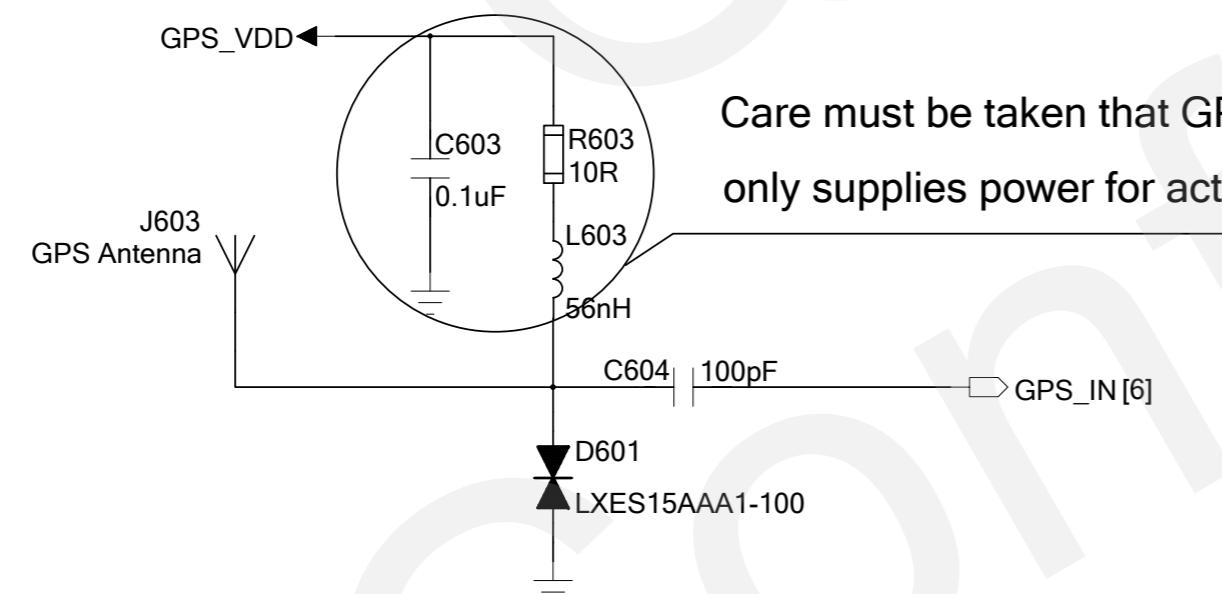
Notes:

1. R603 is designed with GPS antenna short-circuit protection function, which can prevent module from being damaged. The rated power of R603 should be up to 1W.

2. The GNSS-capable antenna is needed to support both GPS and GLONASS system in the future.

3. Customer can use one GPIO to turn on and off the LNA U601 to save the power.

4. The GNSS-capable front-end LNA is needed to support both GPS and GLONASS system in the future.

| Quectel Wireless Solutions		
DRAWN BY <Mountain.ZHOU>	PROJECT <UC20&M10 Reference Design>	TITLE <RF and GPS Design>
CHECKED BY <Bruce.YU>	SIZE A2	VER 1.01
	SHEET 6 of 8	<2013.04>

Other Designs

Indicator

VBAT

D701

For UC20 STATUS application

R701
2.2K

R702
0R

[2] STATUS

Q701
NM

For M10 STATUS application

VBAT

D702

R703
2.2K

[2]NET_MODE

Q702
DTC043ZEBTL

VBAT

D703

R704
2.2K

[2] NET_STATUS

Q703
DTC043ZEBTL
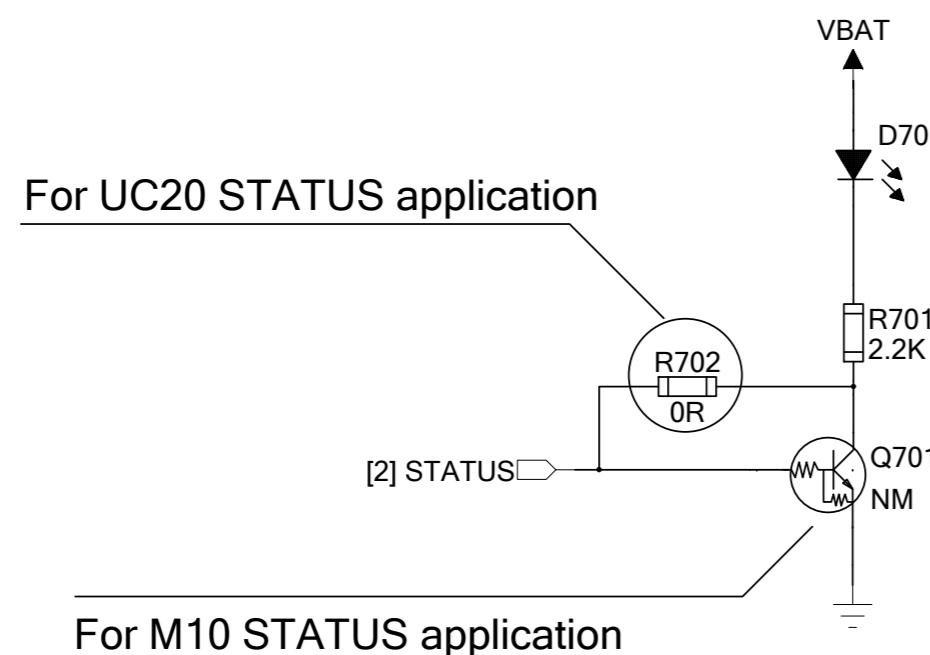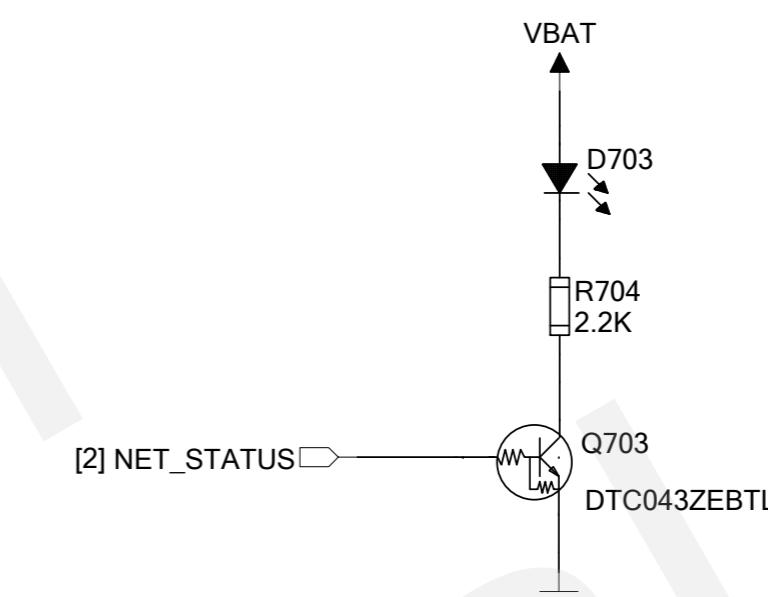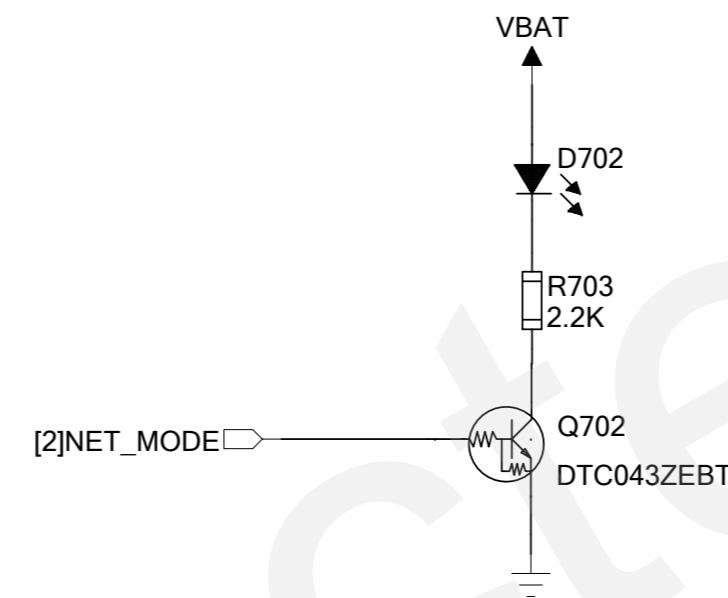
Note:

Refer to the document <UC20_Hardware_Design> for more details about NET_MODE and NET_STATUS.

Reserved Testpoints

U701

|	
1	VBAT [3,7]
2	
3	PWRKEY [2]
4	BOOT_KEY [2]
5	USB_VBUS [2,8]
6	USB_DM [2,8]
7	USB_DP [2,8]
8	TXD [2,4]
9	RXD [2,4]
10	DBG_TXD [2]
11	DBG_RXD [2]

Notes:

1.USB and BOOT_KEY pins are used to upgrade UC20 firmware.

BOOT_KEY needs to be pulled high before upgrading, and keep open in normal mode.

Refer to the document <UC20_Hardware_Design> for more details about BOOT_KEY.

2.M10 upgrades firmware via main UART port (TXD/RXD).

3.Debug UART pins can only be used to catch log.

4.It is recommended to add ESD protection components (e.g. ESDA6V8AV6) on these

reserved testpoints. In addition, the ESD diodes used on USB data lines should have

less than 2 pF of capacitance.

ADC Design

VDD_3V3

R705
10K

R706
10K

D704
PESD5V0S1BL

ADC0 [2]

VDD_3V3

R707
10K

R708
10K

D705
PESD5V0S1BL

ADC1 [2]
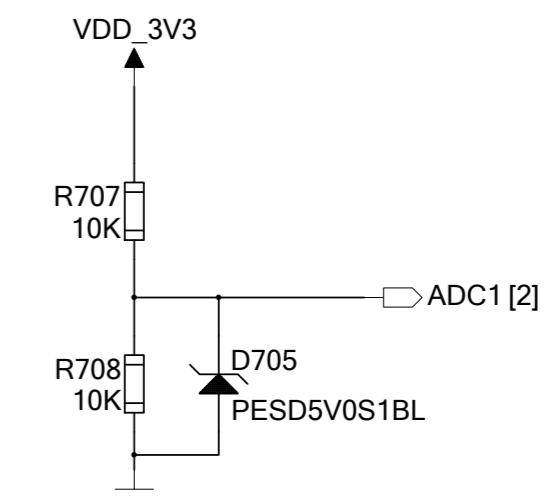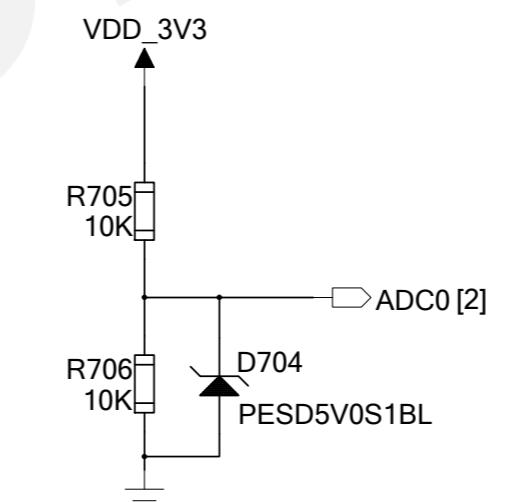
Note:

Input voltage range of UC20 and M10 ADC channels is

0.2~2.1V and 0~2.8V respectively.

MCU Interface

U801

Pin	Signal		Net
1	VDD		VDD_MCU
2	GND		
3	TXD		RXD_M [4]
4	RXD		TXD_M [4]
5	RTS		RTS_M [4]
6	CTS		CTS_M [4]
7	DTR		DTR_M [4]
8	DCD		DCD_M [4]
9	RI		RI_M [4]
10	VBUS	R801 0R	USB_VBUS [2,7,8]
11	VBUS_CONTROL		VBUS_CONTROL [8]
12	USB_DP	R802 0R	USB_DP [2,7]
13	USB_DM	R803 0R	USB_DM [2,7]
14	USB_ID		
15	GPIO_01		ON/OFF_MCU [2]
16	GPIO_02		RESET_MCU [2]
17	GPIO_03		GPS_LNA_EN [6]

MCU

Q801   Si2333CDS-T1

DC_5V   S   D   USB_VBUS[2,7,8]

R804
10K   G

[8] VBUS_CONTROL   Q802
DTC043ZEBTL
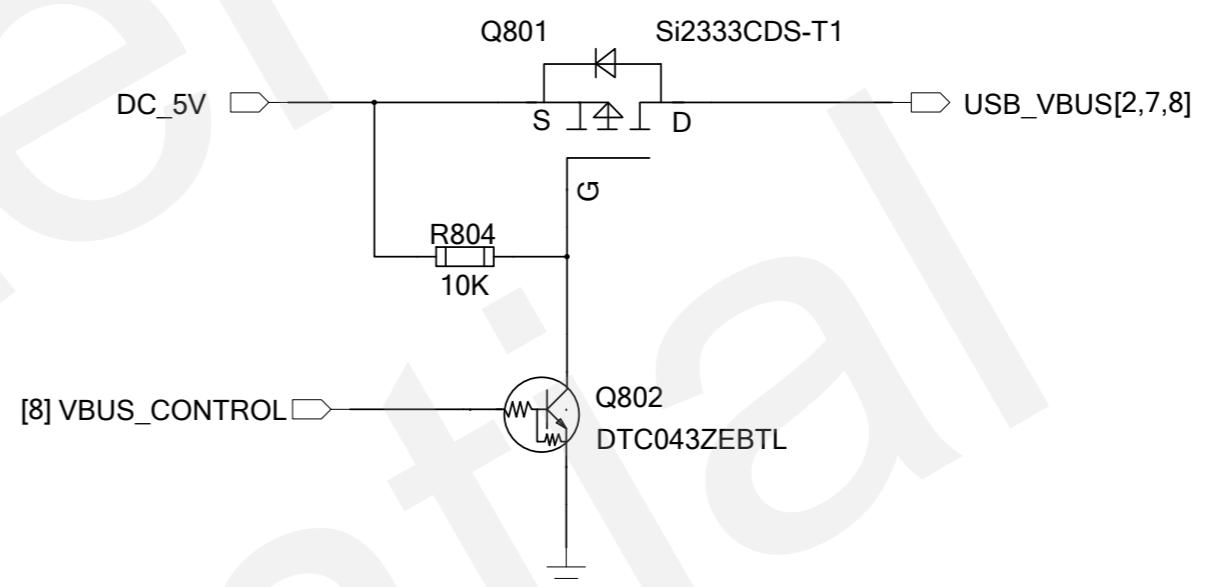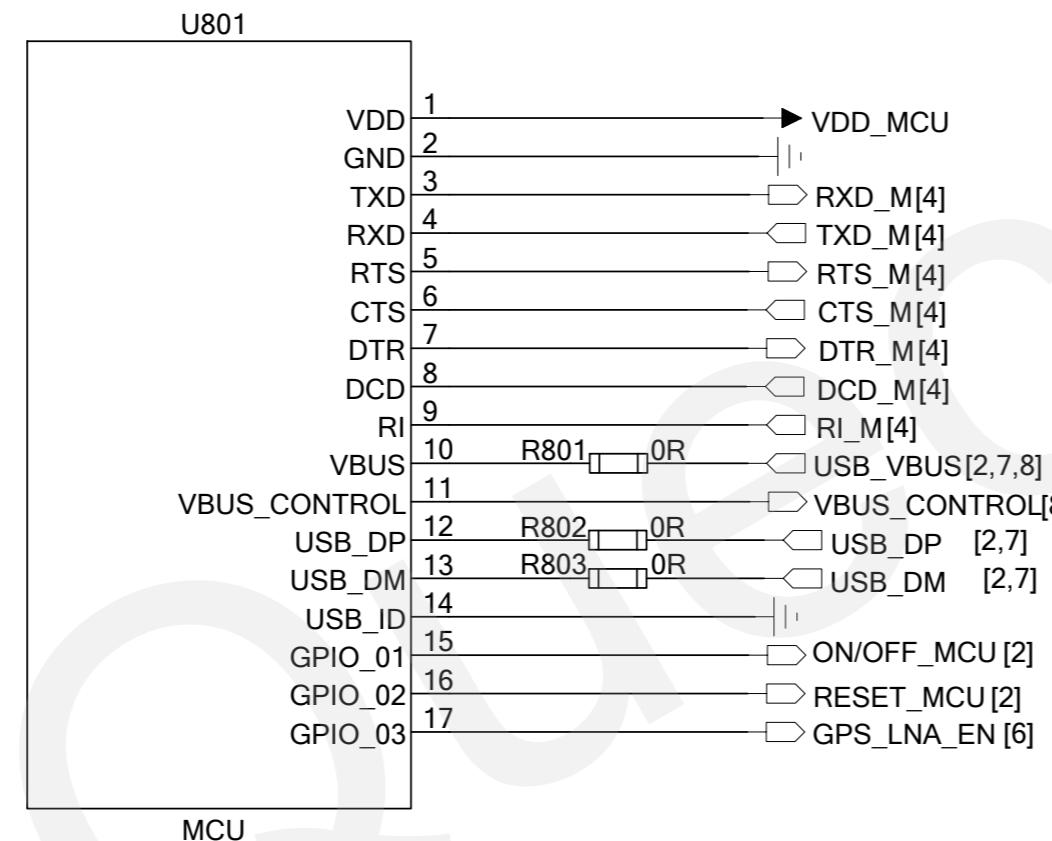
VBUS_CONTROL = High level, Q801 conducts.

Notes:

1.U801 represents customer's MCU.

2.Pay attention to the UART connection of RTS/CTS.

3.UC20 can only work as a USB device and supports LS/FS/HS mode. To communicate with USB interface, MCU needs to support USB host or OTG function.
The VBUS pin of MCU and UC20 need to be provided 5V power for detection, and VBUS_CONTROL turns on and off VBUS power supply.

4.Customers can determine to use USB or UART communication according to their needs.

Application	Installed	Not installed
USB	R801~R804, Q801~Q802	U401 circuit
UART	U401 circuit	R801~R804, Q801~Q802

5.Please pay attention to GPS_LNA_EN voltage level translation for GPS LNA if MCU's GPIO is 5V voltage domain.